



PESD24VV2BT-Q

Bidirectional double ESD protection diode

22 May 2023

Product data sheet

1. General description

Bidirectional double ElectroStatic Discharge (ESD) protection diode in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package designed to protect two data lines from the damage caused by ESD and other transients.

2. Features and benefits

- Reverse stand-off voltage: $V_{RWM} = 24\text{ V}$
- Low clamping voltage: $V_{CL} = 33\text{ V}$ at $I_{PPM} = 3.5\text{ A}$
- ESD protection up to 30 kV (IEC 61000-4-2)
- Ultra low leakage current: $I_{RM} = 1\text{ nA}$
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

ESD protection for low-speed interfaces in automotive, communication, consumer and computing devices.

4. Quick reference data

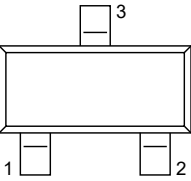
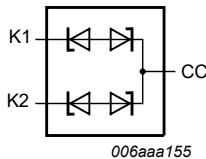
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ °C}$		-	-	24	V
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	14	17	pF

[1] Measured from pin 1 or 2 to pin 3.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p style="text-align: center;">SOT23</p>	 <p style="text-align: center;">006aaa155</p>
2	K2	cathode (diode 2)		
3	K	common cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD24VV2BT-Q	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD24VV2BT-Q	FL%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

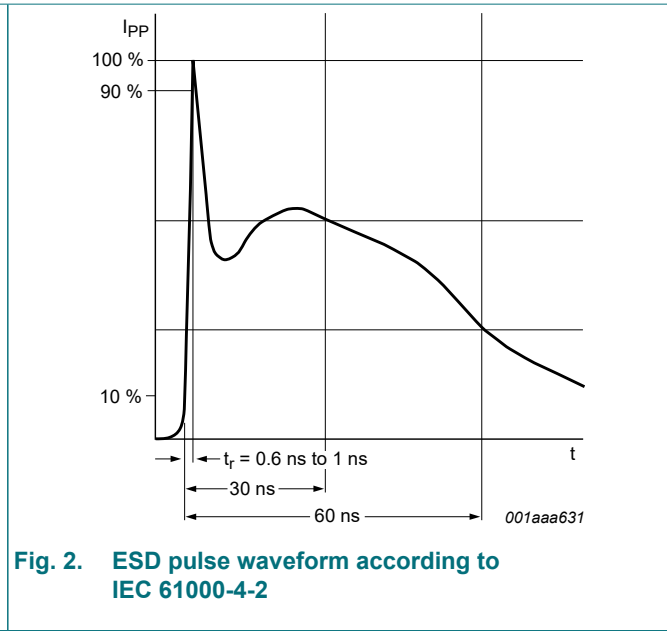
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1] [2]	-	3.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	-	30	kV
		IEC 61000-4-2; air discharge	[2] [3]	-	30	kV

[1] According to IEC 61000-4-5.

[2] Measured from pin 1 or 2 to pin 3.

[3] Device stressed with ten non-repetitive ESD pulses.



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C	-	-	24	V
V _{BR}	breakdown voltage	I _R = 10 mA; T _{amb} = 25 °C	[1]	25.5	30.5	35.5 V
I _{RM}	reverse leakage current	V _{RWM} = 24 V; T _{amb} = 25 °C	[1]	-	1	50 nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	[1]	-	14	17 pF
V _{CL}	clamping voltage	I _{PP} = 1 A; t _p = 8/20 μs; T _{amb} = 25 °C	[2] [1]	-	31	40 V
		I _{PPM} = 3.5 A; t _p = 8/20 μs; T _{amb} = 25 °C	[2] [1]	-	33	42 V
		I _{PP} = 16 A; t _p = TLP; T _{amb} = 25 °C	[3] [1]	-	32	- V
R _{dyn}	dynamic resistance	I _R = 10 A; T _{amb} = 25 °C	[3] [1]	-	0.2	- Ω

[1] Measured from pin 1 or 2 to pin 3.

[2] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

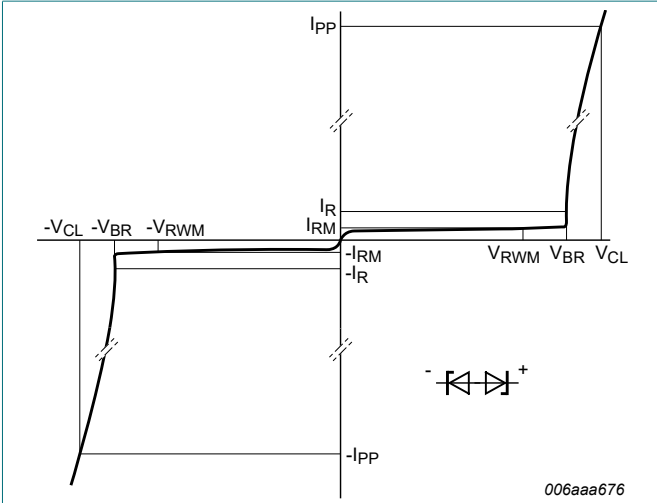


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

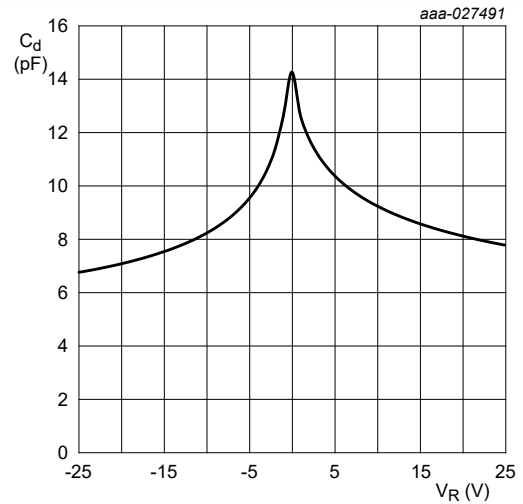


Fig. 4. Diode capacitance as a function of reverse voltage; typical values

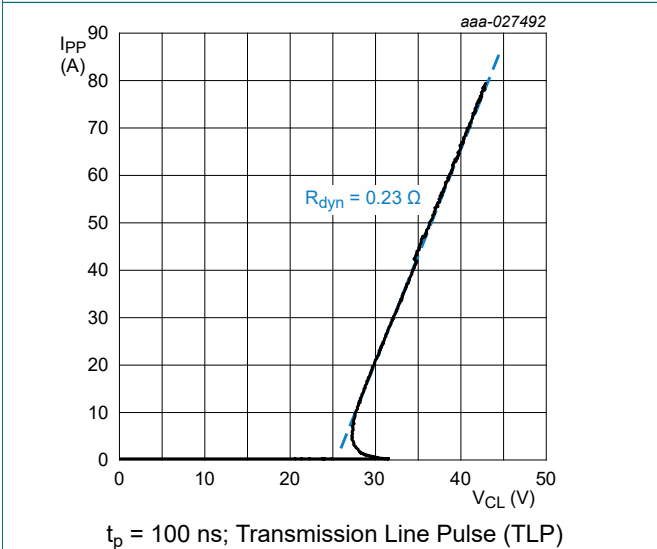


Fig. 5. Positive clamping voltage (TLP); typical values

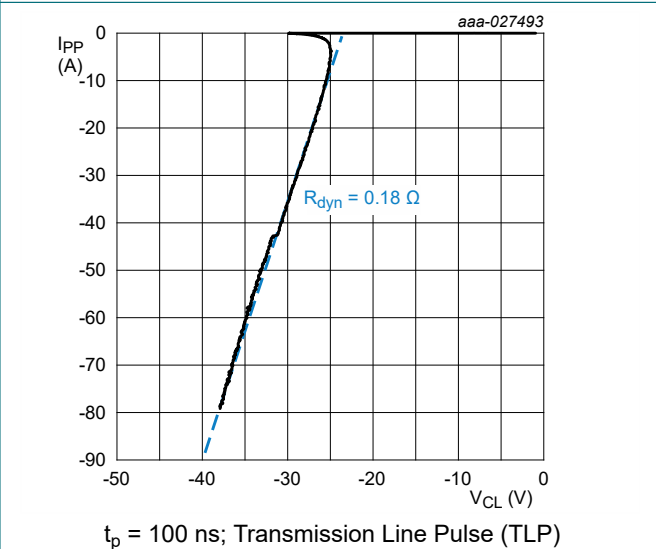


Fig. 6. Negative clamping voltage (TLP); typical values

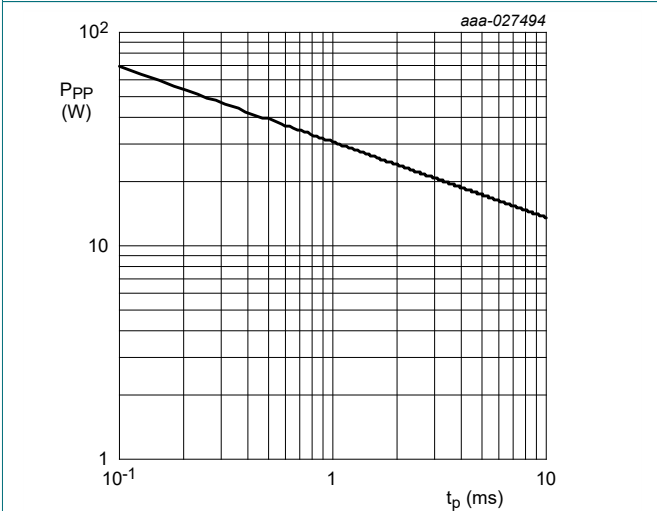


Fig. 7. Peak pulse power as a function of exponential pulse duration; typical values

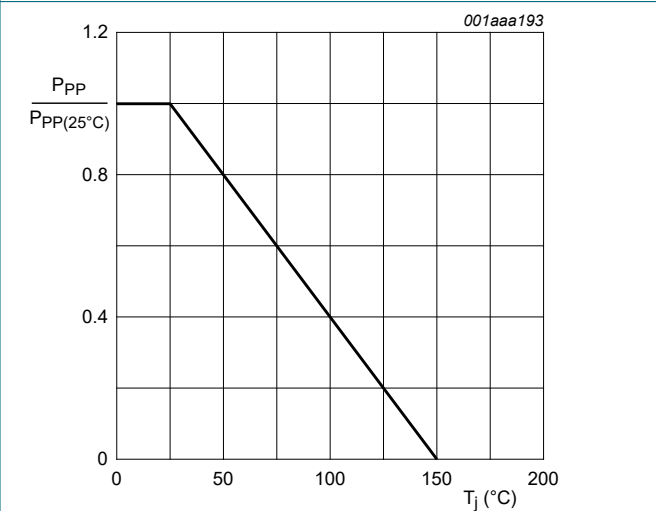
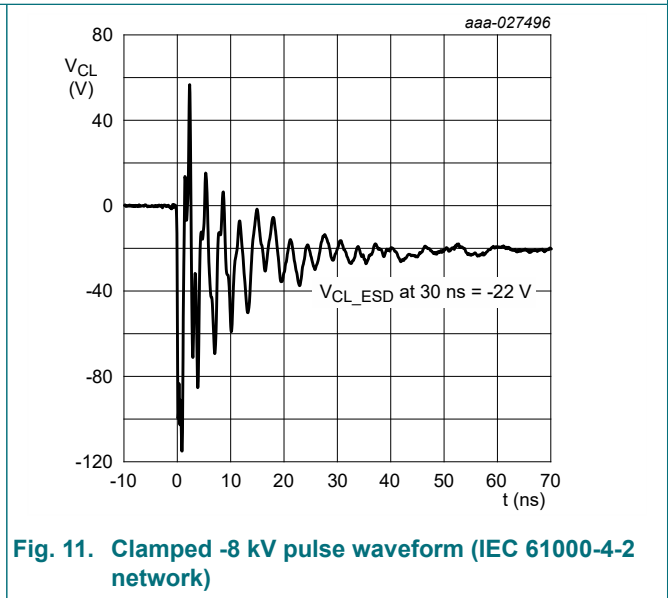
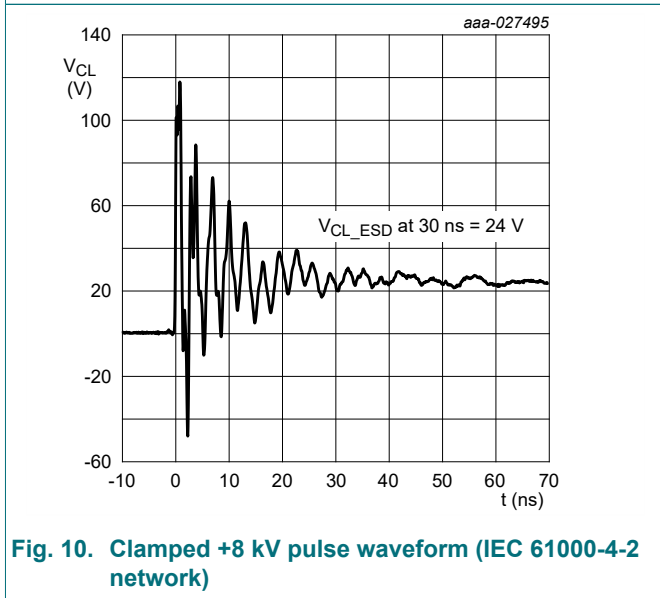


Fig. 8. Relative variation of peak pulse power as a function of junction temperature; typical values



Fig. 9. ESD clamping test setup and waveforms



10. Application information

The device is designed for the protection of two lines from the damage caused by ESD and surge pulses.

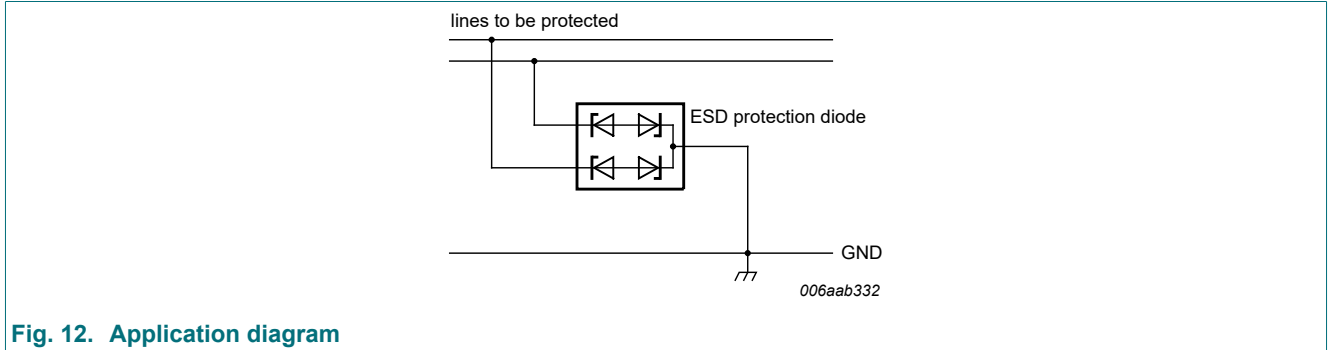


Fig. 12. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

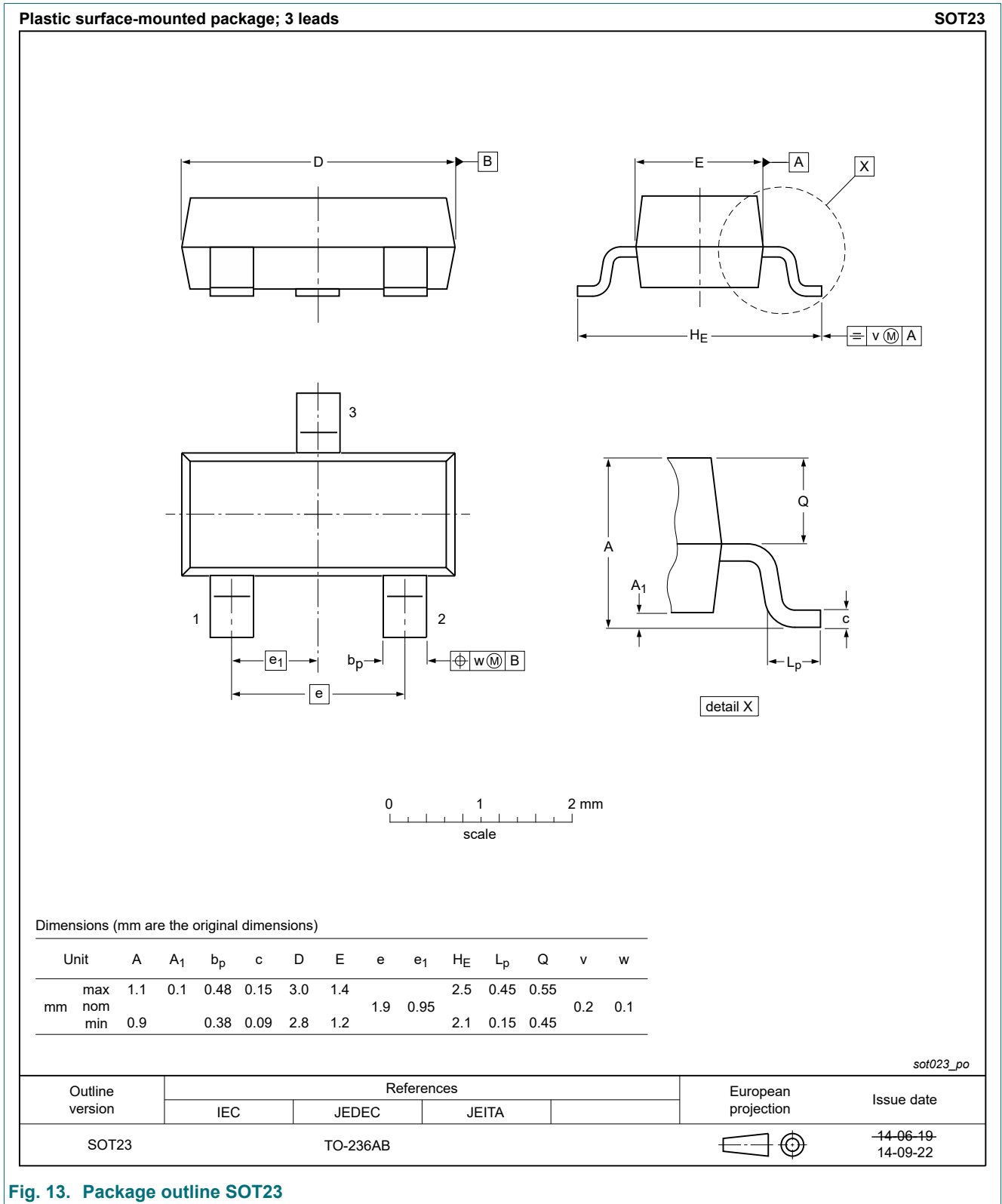


Fig. 13. Package outline SOT23

13. Soldering

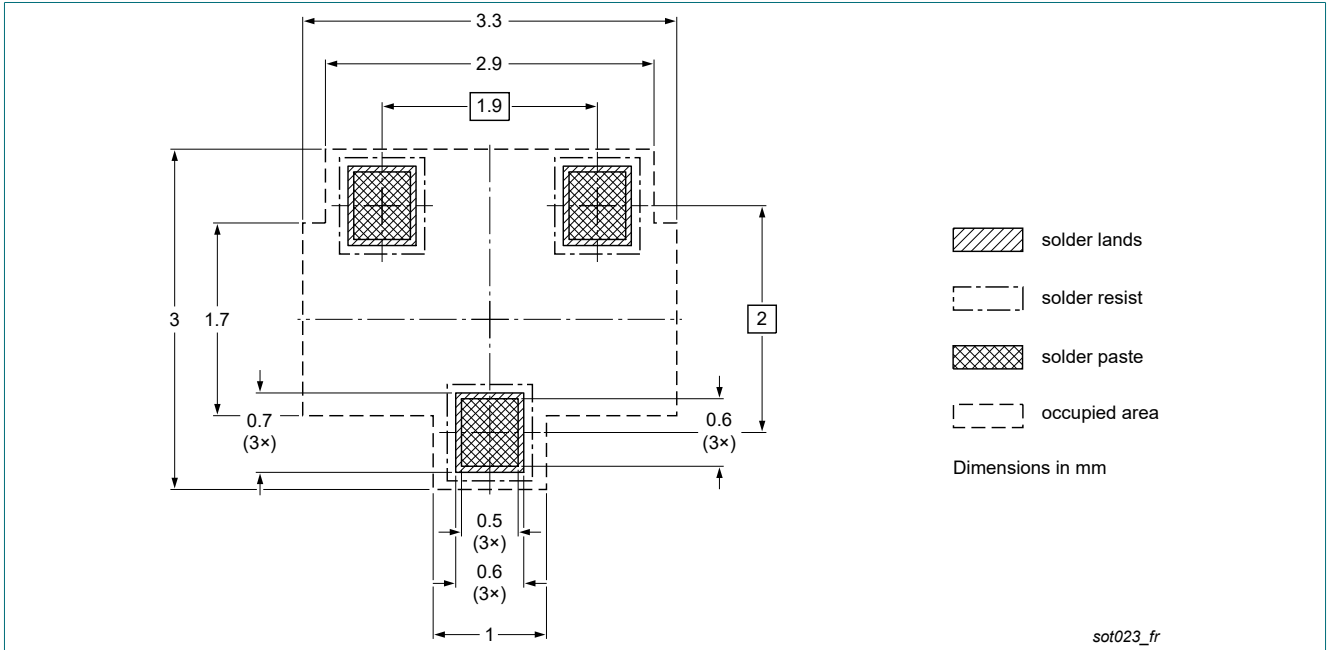


Fig. 14. Reflow soldering footprint for SOT23

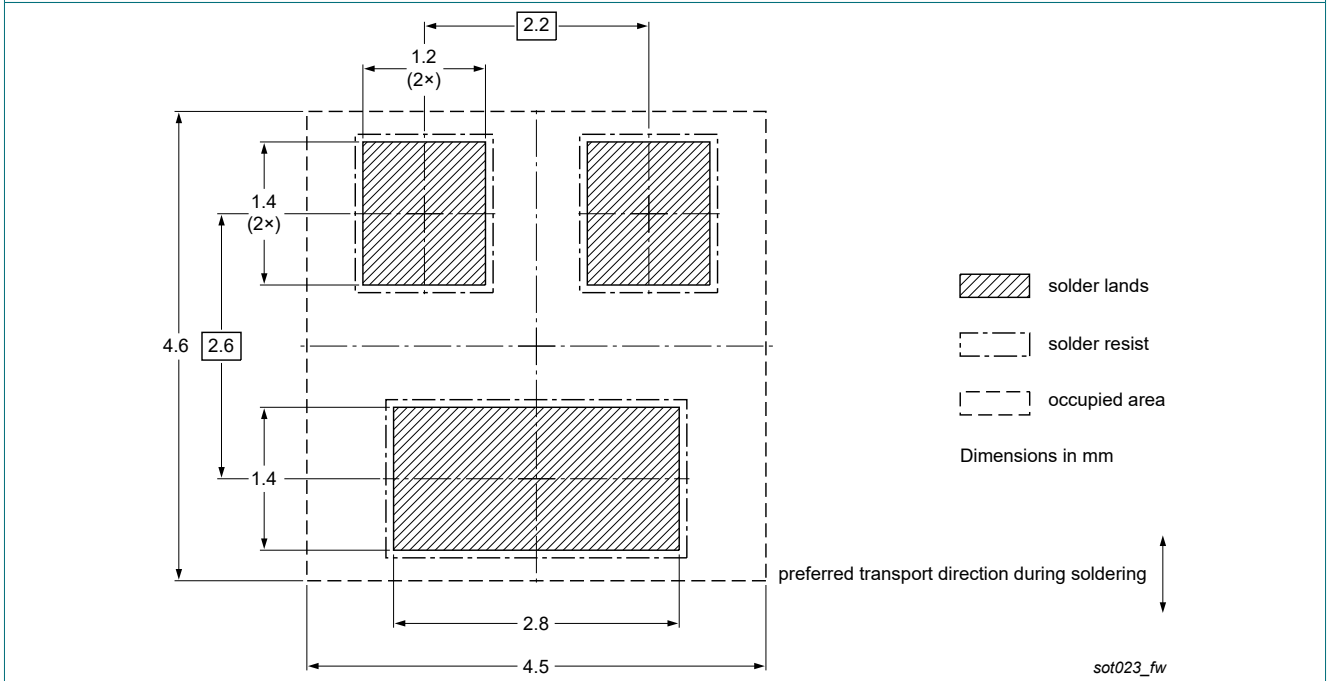


Fig. 15. Wave soldering footprint for SOT23

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD24VV2BT-Q v.1	20230522	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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